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Sheet 1 of 1

FORM PTO-1449 (SUBSTITUTE)		Attorney Docket No.: J&R-0694	Applic. No. 09/922,479
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		Applicant Thomas Zettler	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))		Filing Date August 3, 2001	Group Art Unit 2133

U.S. PATENT DOCUMENTS

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
<i>One</i>	A	4,961,053	10/02/90	Krug			
<i>↑</i>	B	5,355,081	10/11/94	Nakata et al.			
<i>One</i>	C	6,557,130 B1	04/29/03	Krasser et al.			
	D						RECEIVED
	E						DEC 04 2003
	F						Technology Center 2100
	G						
	H						
	I						

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES NO
<i>One</i>	J	0 974 847 A2	01/26/00	Europe			X
<i>One</i>	K	2000 137 059	05/16/00	Japan			X
	L						
	M						
	N						

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	O	
	P	

EXAMINER *One* DATE CONSIDERED *6/26/04*

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609;
Draw line through citation if not in conformance and not considered. Include copy of this form with
next communication to applicant.



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Sheet 1 of 1

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PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE
STATEMENT BY APPLICANT
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Thomas Zettler

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
qme	A	5,241,266	08/31/93	Ahmad et al.			
qme	B	5,388,104	02/07/95	Shirotori et al.			
qme	C	5,570,374	10/29/96	Yau et al.			
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DEC 06 2001

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES NO
qme	J	0 492 624 A1	07/01/92	Europe			X
qme	K	0 568 239 A2	11/03/93	Europe			X
qme	L	00 124 279 A	04/28/00	Japan			X
	M						
	N						

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

qme	O	Rangarajan, Sampath et al.: "Built-In Testing of Integrated Circuit Wafers", IEEE Transactions on Computers, Vol. 39, No. 2, February 1990, pp. 195-205
	P	

EXAMINER	DATE CONSIDERED
<i>qme</i>	6/26/04

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